CLAIMS

What is claimed is:

1. A lead frame of a plurality of lead frames, said lead frame for a semiconductor device having a first surface having at least one bond pad located thereon and having a bottom surface, said lead frame comprising:

a lead frame of a plurality of lead frames, each lead frame located adjacent another lead frame having an opening located therebetween;

a plurality of lead fingers of said lead frame, each lead finger of the plurality having an end, at least a portion of the plurality of lead fingers having an opening for locating a semiconductor device therein;

at least one bus bar having a portion extending along an end of at least one lead finger of the plurality of lead fingers, said at least one bus bar including a first portion extending along the end of the at least one lead finger of the plurality of lead fingers; and

a section of tape substantially rectangular in shape having an outer peripheral portion and a central portion for attaching at least a portion of said first surface of said semiconductor device thereto, the outer peripheral portion of the section of tape for attaching at least a portion of at least two ends of the lead fingers of the plurality of lead fingers thereto, the section of tape being attached to a portion of the at least one bus bar.

2. The lead frame of claim 1, wherein the lead frame includes at least two bus bars, each bus bar of the at least two bus bars having a longitudinal contact portion extending along the end of said at least one lead finger of the plurality of lead fingers.

3. The lead frame of claim 1, wherein the at least one bus bar includes said first portion extending along said end of at least one lead finger of the plurality of lead fingers.

4. A lead frame of a plurality of lead frames for connecting a semiconductor device thereto having a periphery, said lead frame comprising:

a lead frame of a plurality of lead frames, each lead frame located adjacent another lead frame having an opening therebetween;

a plurality of lead fingers of said leaf frame, each lead finger of the plurality of lead fingers having an end, at least a portion of the plurality of lead fingers defining a semiconductor device opening in the lead frame;

a die paddle for supporting a semiconductor device thereon; and

at least two bus bars, each having at least a portion thereof extending along at least portions of two adjacent portions of said periphery of said semiconductor device, said at least two bus bars having a first portion thereof extending along the end of the each lead finger of the plurality of lead fingers.

5. A lead frame of a plurality of lead frames for use with a semiconductor device having a periphery, said lead frame comprising:

a lead frame located adjacent another lead frame of a plurality of lead frames having a n opening therebetween, said lead frame having a plurality of inwardly extending leads to an opening for said semiconductor device, at least one lead of said plurality of inwardly extending leads having a portion extending along at least a portion of a length of at least two adjacent portions of said periphery of said semiconductor device and extending between said semiconductor device and another lead of said plurality of inwardly extending leads and a second extending lead extending along another portion of the length of the periphery of said semiconductor device, said at least one lead of said plurality of inwardly extending leads electrically connects said semiconductor device to a power source.

6. The lead frame of claim 5, wherein said at least one lead of said plurality of inwardly extending leads electrically connects said semiconductor device to a ground.

7. The lead frame of claim 5, wherein said at least one lead of the plurality of inwardly extending leads electrically connects said semiconductor device to a reference voltage.

8. The lead frame of claim 5, wherein said at least one lead of the plurality of inwardly extending leads substantially surrounds said at least two adjacent sides of said plurality of sides of said periphery of said semiconductor device.

9. The lead frame of claim 5, wherein said at least one lead of the plurality of inwardly extending leads is bifurcated.

10. The lead frame of claim 9, wherein a first portion of said at least one inwardly extending bifurcated lead extends along a first portion of the periphery of said semiconductor device and a second portion of said at least one inwardly extending bifurcated lead extends along another adjacent portion of the periphery of said semiconductor device.

11. The lead frame of claim 5, further comprising:

a second extending lead extending along another portion of length of the periphery of said semiconductor device.

12. The lead frame of claim 5, wherein said at least one lead of the plurality of inwardly extending leads extends along a portion of the periphery of said semiconductor device and said second extending lead extends along another opposite portion of the periphery of said semiconductor device.

13. The lead frame of claim 12, wherein said at least one lead of the plurality of inwardly extending leads substantially surrounds said semiconductor device and said second extending lead substantially surrounds said semiconductor device.

14. The lead frame of claim 12, wherein said at least one lead of the plurality of inwardly extending leads and said second extending lead are bifurcated forming a first portion and a second portion on said at least one lead of the plurality of inwardly extending leads and a first portion and a second portion on said second extending lead.

15. The lead frame of claim 14, wherein said first portion of said at least one bifurcated, inwardly extending lead extends along a first portion of the periphery of said semiconductor device and said second portion of said at least one bifurcated, inwardly extending lead extends along a second portion of the periphery of said semiconductor device and said first portion of said second bifurcated, inwardly extending lead extends along a third portion of the periphery of said semiconductor device and said second portion of said second bifurcated, inwardly extending lead extends along a fourth portion of the periphery of said semiconductor device.